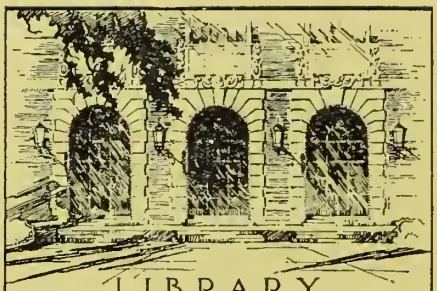

Math

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DESIGN OF A HIGH SPEED A/D CONVERTER

by

ARTHUR SIMONS

JUNE, 1968

DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

Report No. 269

DESIGN OF A HIGH SPEED A/D CONVERTER*

by

ARTHUR SIMONS

June, 1968

Department of Computer Science
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Urbana, Illinois 61801

* Submitted in partial fulfillment for the degree of Master of Science in Electrical Engineering, at the University of Illinois, June, 1968.

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The author wishes to express his gratitude to his advisor, Professor W. J. Poppelbaum, whose counsel and encouragement have been very helpful.

Special thanks are also extended to the other members of the Functional Encoding Project; Peter Oberbeck, whose guidance throughout the construction of the system was invaluable, and Edward Carr, who did a large share of the work on the Sample-and-Hold circuit.

PREFACE

Since A/D converters are not used by themselves, it is necessary to describe the system for which the converter is built to see what is required of the converter in terms of cost, size, speed, and accuracy.

The Functional Encoding System, conceived by Professor W. J. Poppelbaum, is a research project concerned with transmitting line drawings over a bandwidth considerably smaller than the standard bandwidth of TV systems. The internal hardware, designed and built by Peter Oberbeck, Edward Carr, and the author, comprises analog, digital, and hybrid circuits. One of the hybrid circuits needed for the system was a very fast analog-to-digital converter; the author's Master's Degree project was to design and construct the A/D converter.

The first part of this thesis is a brief introduction to the Functional Encoding System, followed by a general description of the design of some common A/D converters. Chapter 2 describes the system design of the converter and Chapter 3 deals with the technical design of all the circuitry involved in the construction of the converter. The thesis is concluded with a discussion of the significance of this particular A/D converter design in relation to the state of the art of the electronics industry.

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1. INTRODUCTION

1.1 Functional Encoding

Conventional TV systems of the broadcast type have a bandwidth requirement of 4.2 MHz. This 4.2 MHz bandwidth is used regardless of the complexity of the picture, whether it is a simple black and white line drawing or a complex scene containing several shades of grey.

Intuitively, one would suspect that the simple line drawing could be transmitted over a bandwidth considerably smaller than 4.2 MHz.

Suppose a line drawing is being picked up by a camera and displayed on a TV monitor as shown in Figure 1. The video signal from each of the 525 scans will have a transition at each intersection of the horizontal scan with the lines on the screen. A sample of video is shown in Figure 2. The positive transitions indicate the intersections.

Then, the elapsed time between these transitions can be encoded into voltage levels. These voltage levels would be transmitted at a rate of (15.75) N KHz, where N is the number of functions to be transmitted. Figure 3 shows how a single scan line of video corresponding to a four-line drawing (N=4) is encoded. One can see how the elapsed time between intersections of the horizontal scan and the lines on the drawing are encoded into voltage levels spaced at $63.5/N$ μ second intervals. The elapsed times between these intersections may be very small, and hence have a high frequency content in the original video signal. The encoded signal after integration, however, does not have these high frequency signals.

There are two major devices in the system: one is the encoder or transmitter; the other is the decoder or receiver. In the description

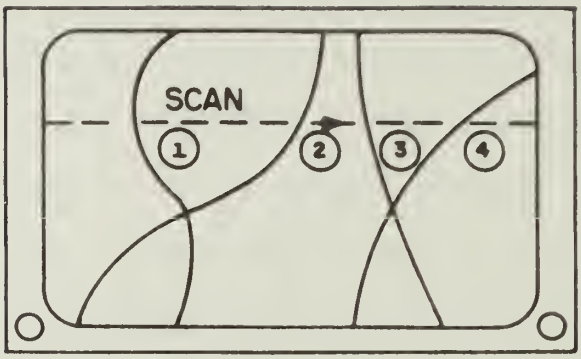


Figure 1. Line Drawing on TV Monitor with Sample Scan.

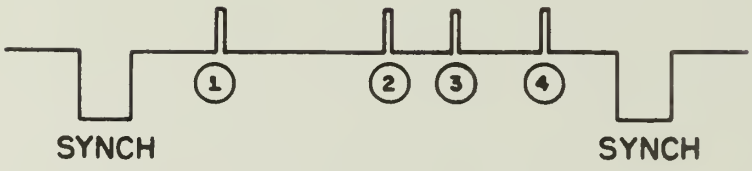


Figure 2. Video Signal from Sample Scan of Figure 1.

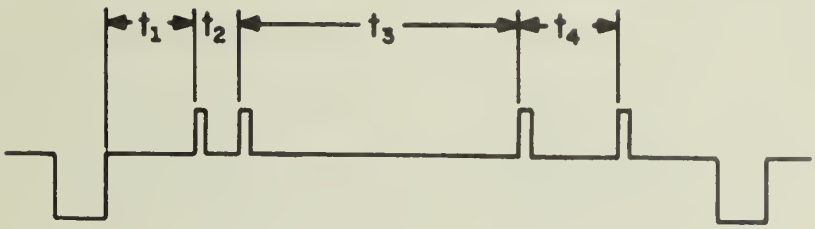


Figure 3a. Video Signal.

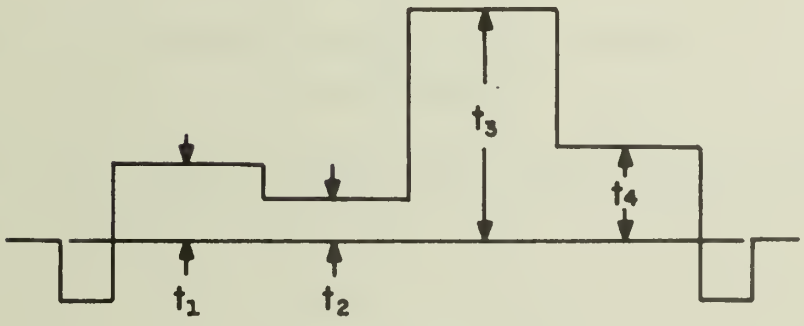


Figure 3b. Encoded Video Signal.

of the transmitter, reference to Figure 4 will help in the understanding of the system.

A master clock running at 9.45 MHz divides each horizontal line into 512 positions. Each time the horizontal scan intersects a line on the drawing, a sharp pulse is noted on the video of the camera. These pulses are used to start and stop, sequentially, the 32 9-bit counters. The contents of each counter will then represent the elapsed time between video pulses, or distance between lines on the drawing. At the end of each scan the contents of these counters are gated into a set of 32 9-bit registers, themselves gated sequentially to a D/A converter whose output is then the encoded video signal.

A block diagram of the receiver is shown in Figure 5. The encoded video signal is received and sampled to determine the amplitude of the incoming pulses. The rate of sampling is determined by the number of intersections which are being transmitted. The sampled video is then fed into the A/D converter. Since a maximum of 32 horizontal intersections may be received during a line time of approximately 52 μseconds, the rate of information into the A/D converter can be as fast as once every 1.6 μseconds.

The transmitted analog signal from encoder to decoder can be from 0 to +5.0 volts. Therefore, the least significant bit of the 9-bit A/D converter represents an analog signal of less than 10mv.

The receiver for this system will be housed in a cabinet with almost all of the circuitry integrated and built on printed circuit boards. Due to the large number of integrated circuits used in the system, both the size and cost of the A/D converter is restricted. It is desired that the entire A/D converter be built on less than 10

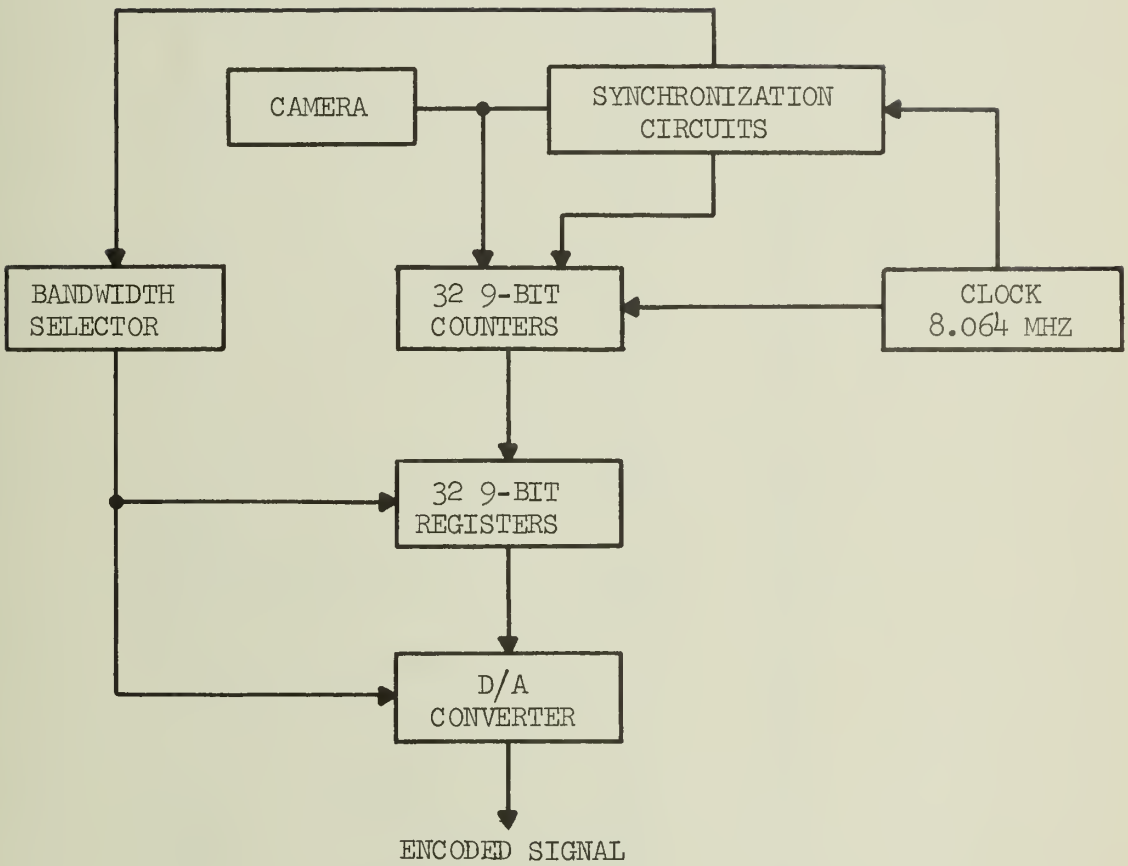


Figure 4. Block Diagram of Functional Encoding Transmitter.

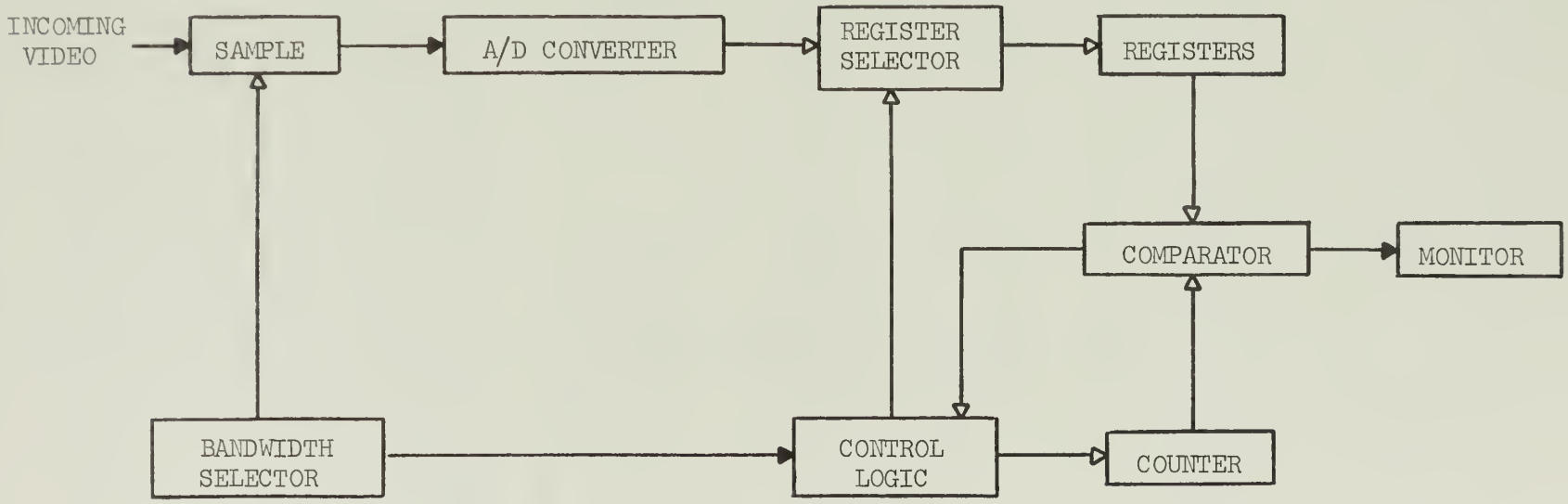


Figure 5. Block Diagram of Functional Encoding Receiver.

printed circuit boards. Furthermore, the components used in the A/D converter designed for the system cost less than $2000.00 - nearly 5 times cheaper than commercially available converters that do not even fulfill the conversion speed requirements.

1.2 A/D Converters

So far as a digital system is concerned, all A/D converters do the same thing: they convert an analog voltage to a digital number. However, for practical reasons it could be useful to break the class of A/D converters into several subclasses.

Synchro, or resolver to digital converters, are single-channel units, but they convert the three-wire signals of a synchro or the four-wire signals of a resolver into a digital number representation of shaft angle.

Analog-to-digital encoders are essentially converters of shaft angle. Since each encoder is mechanically linked to a specific shaft, they cannot be multiplexed and normally you need one encoder per channel.

Linear or single-function A/D's convert a single analog voltage to a digital number. Converters of this type can measure the output voltage of a thermo couple, the output of a pressure transducer and similar variables.

Obviously, for this system we are interested in designing a single-function A/D converter. It simply must convert the transmitted analog video signal to a 9-bit digital number quickly enough to enable the receiver to function and transmit pictures in real time.

Many A/D conversion techniques have been developed. An extensive study of these ideas was the first step in designing the A/D converter. Foremost among the methods in common use are the following:

1) Simultaneous Method - Figure 6a shows how a simple simultaneous analog-to-digital converter can be built using several comparator circuits. The basis of A/D conversion is the comparator circuit. This circuit compares an unknown voltage with a reference voltage and indicates

C_1	C_2	C_3	Input Voltage
off	off	off	0 to V/4
on	off	off	V/4 to V/2
on	on	off	V/2 to 3V/4
on	on	on	3V/4 to V

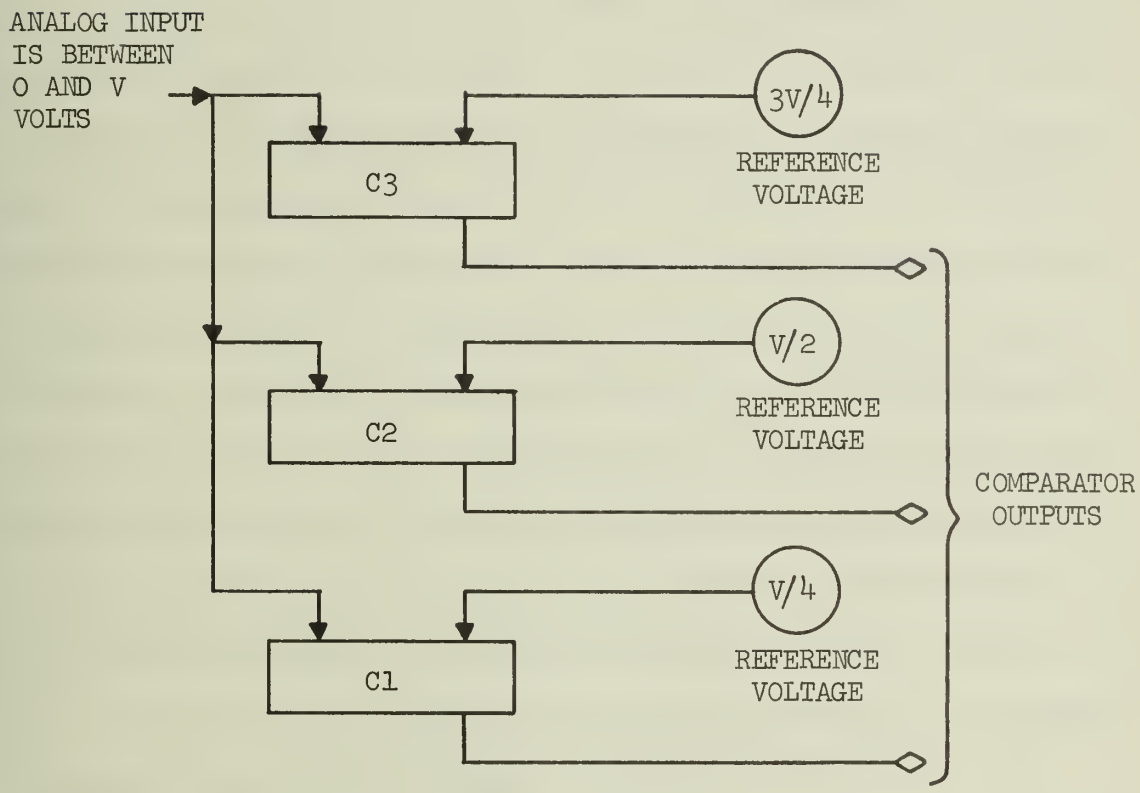


Figure 6a. Simultaneous Converter

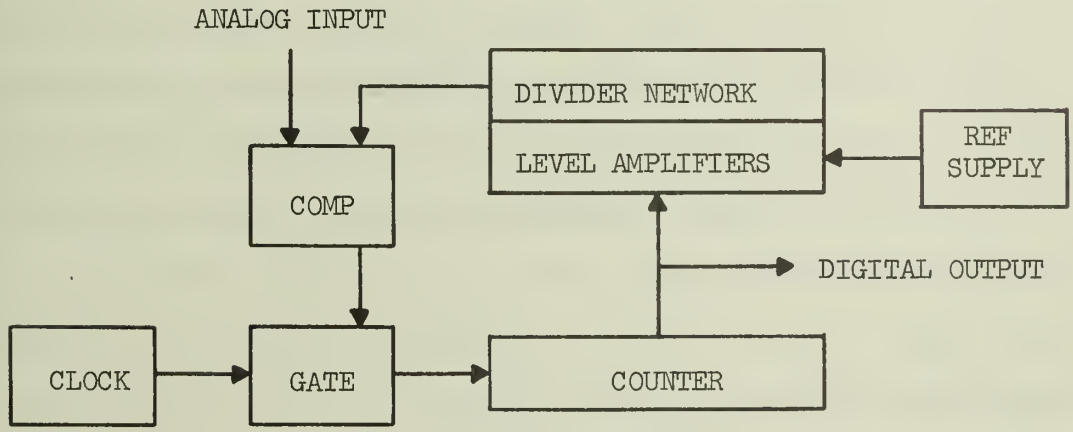


Figure 6b. Counter Converter

which of the two is larger. Each comparator has a reference input signal. The other input terminal of the comparators is between 0 and V volts. The comparator is called "on" if the analog input is larger than the reference input. Then, if none of the comparators are on, the analog input must be less than V/4. If C-1 is on, and C-2 and C-3 are off, the input must be between V/4 and V/2. Similarly, if C-1 and C-2 are on, and C-3 off the voltage is greater than 3V/4; and if all the comparators are on, the voltage is greater than 3V/4. Here, the voltage range is divided into four parts which can be coded to give two binary bits of information. In general, 2^N-1 comparators will give N bits of binary information. The simultaneous method is extremely fast for small resolution systems. For large resolution systems, this method requires so many comparators that it becomes unwieldy and prohibitively costly. For our 9-bit converter, this method would require 511 comparators. Not only is this cumbersome and expensive but the problems associated with connecting so many circuits together would probably prove insurmountable.

2) Counter Method - If the reference voltage were variable, only one comparator would be needed. But a digitally controlled variable reference is simply a digital-to-analog converter. With a digital number in the D/A converter the comparator indicates whether the corresponding voltage is larger or smaller than the input. With this information, the digital number is modified and compared again. A simple method is to start at zero and count until the D/A converter equals or exceeds the analog input. Figure 6b shows a converter in which the D/A converter register is a counter, and a pulse source is included. The gate stops pulses from entering the counter when the comparator indicates that the conversion is complete. While the counter method is good for high

resolution systems (as the number of bits is increased, very little additional circuitry is required), conversion time increases rapidly with the number of bits. An N-bit converter must allow time for 2^N counts to accumulate. For our requirements then, it would be necessary to use a counter operating at nearly 500 MHz. This, of course, at present is not possible.

3) Section Counter - The counter converter is a simple technique for performing conversions; however, if the digital word becomes long, the 2^N steps required to complete the conversion may be too many. One way to decrease the time at a minimum of cost is to divide the counter into sections. For example, a 10-bit converter could be divided into two sections of five bits each. At the beginning of the conversion the least significant counter is set to all ones and counts are inserted into the most significant counter until the comparator indicates that the input has been exceeded. The least significant counter is then cleared and counted up until the correct value is reached. The maximum number of steps required to complete a conversion is 2^5 for the most significant counter and 2^5 for the least significant counter, giving a total of 2^6 steps. This is a maximum of 64 counts versus 1024 counts for the standard counter converter. While this technique could reduce considerably the frequency of operation required in the counter, it would still have to operate at approximately 50 MHz. Though not directly practical, the basic idea of separating the conversion process into two distinct portions has definite merits.

4) Ramp Method - In the counter converter, each count input is increasing the voltage out of the DAC by one step, effectively generating a ramp out of the DAC. Thus the level amplifiers, reference supply, and

divider network could be replaced by an external ramp generator circuit. If accuracy is not too important, the ramp can be made by charging a capacitor with a current source and using the linear part of the exponential. In high resolution converters, the ramp might be made by using an operational amplifier as an integrator.

The ramp technique is somewhat faster than the counter technique because carry and DAC set up time is not required before gating the next count pulse. The differential linearity, over a short span of a ramp converter, is bound to be fairly good, since the ramp is a continuous signal. Although there may be some noise, the general slope will not change significantly over a short span.

2. SYSTEM DESIGN

As discussed in section 1.2 many methods for performing an A/D conversion have been developed. However, it is also noted that these techniques were proven too expensive, too unpractical, or just not fast enough for direct use in the project. On the other hand, it was thought that a combination of a few of the basic ideas might suggest a possible scheme.

The importance of the comparator circuit in A/D converter design was also mentioned. During preliminary investigations into different ideas, Fairchild Semiconductor Corporation announced the completion of a new product - an integrated circuit differential voltage comparator - capable of comparing two voltages very accurately in 40 nanoseconds. When this small, inexpensive comparator was tested and found to perform satisfactorily, it was decided to rely heavily upon its use in designing the A/D converter.

One of the most essential parts of the A/D converter, necessarily common to all the ideas which were suggested, was a sample-and-hold circuit. Since all devices for converting analog quantities to digital form require a fixed interval of time to perform the conversion, it is often necessary to insure that the analog input quantity being measured remains fixed throughout the conversion period. In this case the analog input is changing continuously, and at a very high rate. Therefore, it was important to design a sample-and-hold circuit which could sample the input very accurately and very quickly, yet be capable of holding that voltage for a time long enough to allow the converter to perform all its functions.

As a result of combining more than one technique and using the very fast comparator circuit whenever possible, three ideas were proposed; the first two were eventually discarded and the third one agreed upon. A block diagram of the first suggested idea appears in Figure 7. This method utilizes the techniques advanced in the simultaneous method, the counter method, and the section counter (see section 1.2). By determining the total of nine bits in a serial-parallel method a great deal of conversion time could be eliminated. By serial-parallel is meant that first the five most significant bits would be determined at one time, and then the four least significant bits would be determined at one time. Finding the four least significant bits would, of course, be facilitated by the fact that the five other bits were already determined and could be used.

First, a comparison method is used to obtain the five most significant bits. The basis for this technique is the comparator circuit and, in general, to obtain N bits of information, 2^N-1 comparators are needed. Since the comparators work simultaneously, this method is extremely fast. It was decided to determine five bits with this method because the number of comparators is still reasonable (31 are needed), while allowing enough time to determine the remaining four bits. After the 31 digital outputs of the comparators are encoded into the five most significant bits, the four least significant bits are determined by a countdown method. The five most significant bits are shifted into a 9-bit register with the four least significant bits set to zero. These 9-bits are then fed into a digital-to-analog converter, the output of which compared with the original input signal. If they are equal, the process stops and the conversion is completed. However, if the

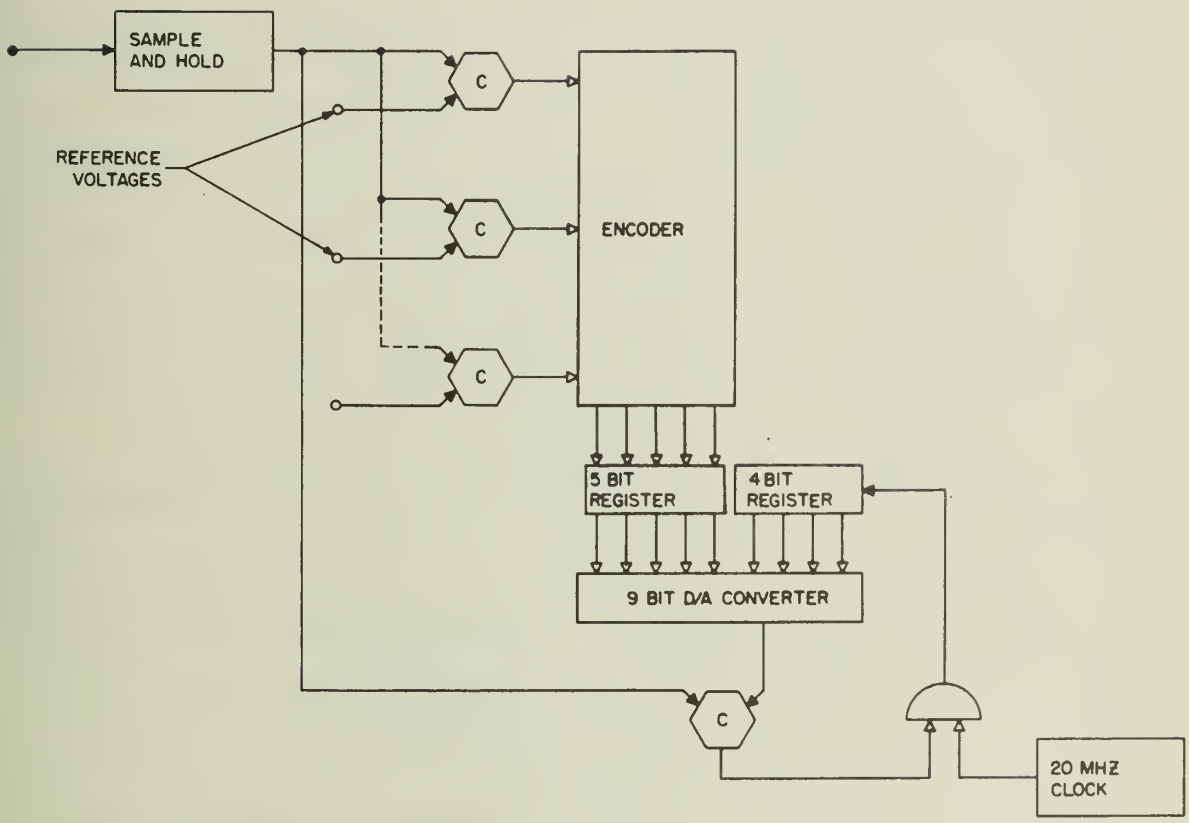


Figure 7. A/D Converter - Type I.

input signal is larger than the D/A conversion of the five most significant bits, a clock is gated into the register until the output of the D/A converter does equal the input signal. The contents of the 9-bit register, at the time the comparator stops further clock pulses from entering, is the desired digital representation of the analog input.

A second method of performing the A/D conversion was suggested and appears in Figure 8. Very similar to the first technique, it utilizes the ramp method instead of the countdown method for determining the four least significant bits. Here the five most significant bits are once again determined by a comparison method, but they are gated into a 5-bit register and then a 5-bit D/A converter. A 4-bit register representing the four least significant bits is again set to zero. If the output of the D/A converter equals the input signal, the process stops. If the input signal is larger than the output of the D/A converter, a clock is gated into the 4-bit register. Simultaneously, a ramp voltage is triggered and added to the output of the D/A converter, and the sum of the two is compared to the input signal. When they are equal the clock is gated off and the output may be taken from the two registers. While the second method does require additional circuitry, it offers the advantage of requiring only one D/A conversion, while the first method requires a conversion every time a clock pulse enters the register. In the first method, as many as sixteen high-speed conversions may be necessary.

At this point both methods were feasible, but neither was exceptionally fast. The final method, seen in Figure 9, is very fast, however. While it was desired that the conversion time be as little as 1.6 μseconds, the converter finally designed is capable of conversion

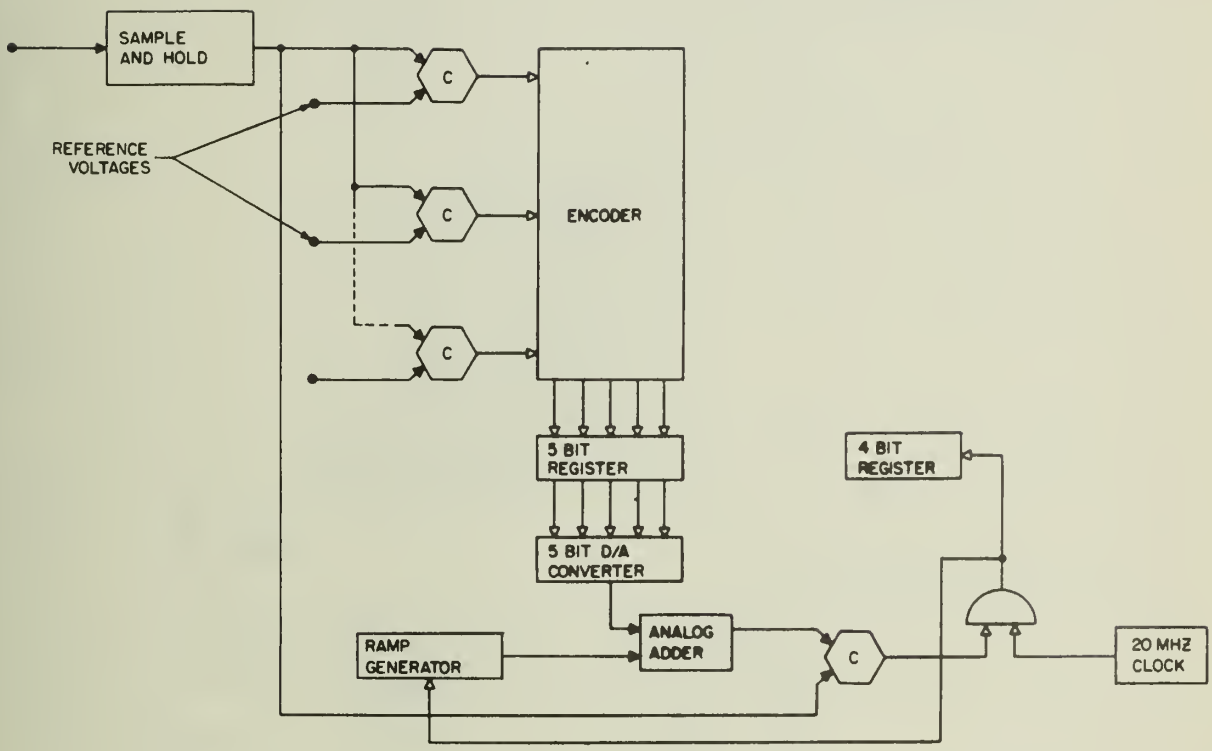


Figure 8. A/D Converter - Type II.

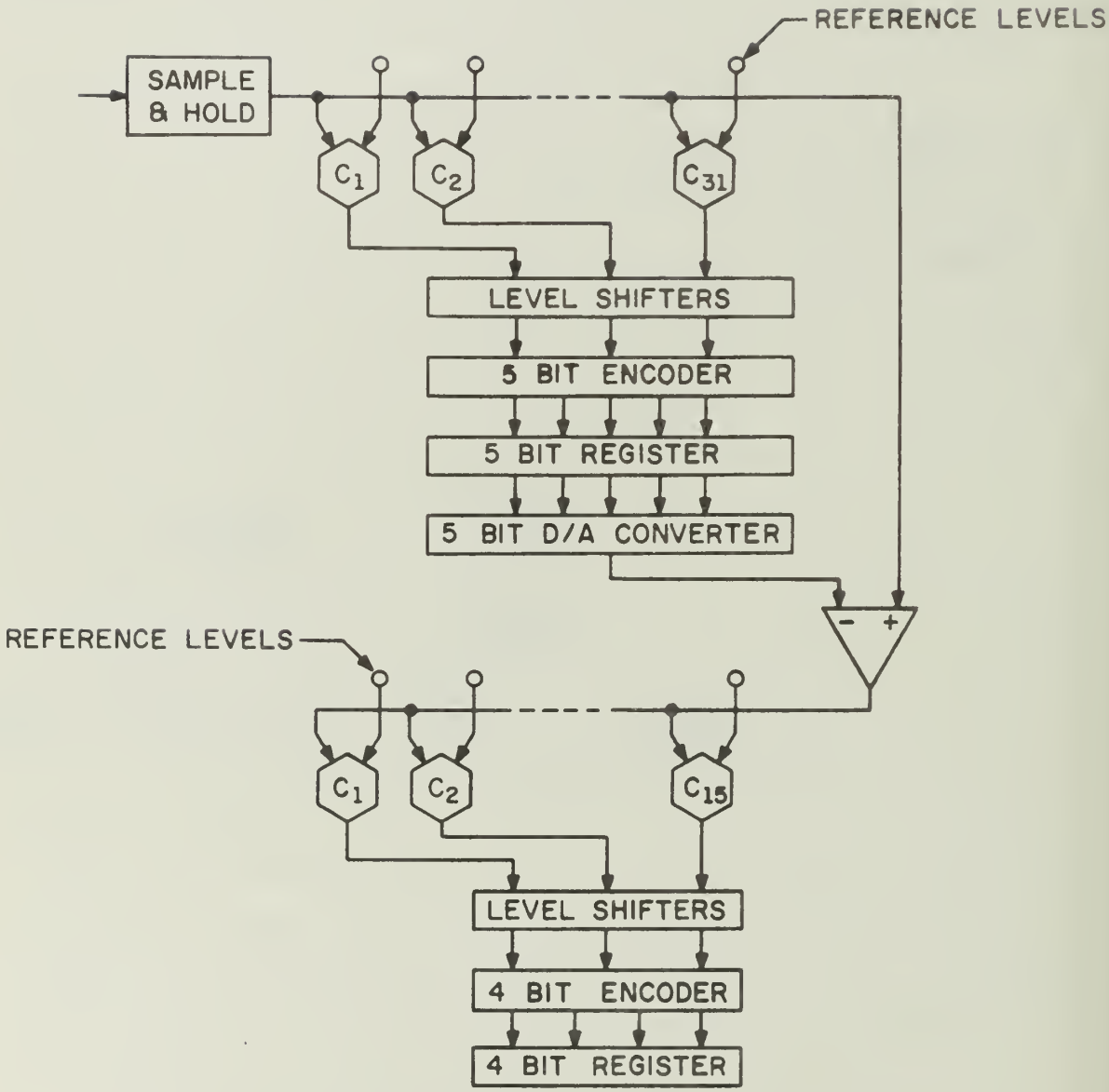


Figure 9. Analog-Digital Converter.

The first two techniques utilized the comparison method for determining the five most significant bits, and then a different method was used to convert the remaining four bits. In the new system, however, the comparison method is used to convert all nine bits. A block diagram of the converter is shown in Figure 9. Once again the five most significant bits are determined by a simultaneous comparison of the input signal with 31 reference voltages and a subsequent encoding of the 31 digital outputs of the comparators. The five bits are then stored in a register and fed into a 5-bit D/A converter. The resulting analog signal, corresponding to the five most significant bits, is then subtracted from the input signal and the resulting signal is converted into four bits in an identical manner. This method is simpler than both previous techniques and, in addition, is much faster.

The logic level converting circuits (see Figure 9) were needed because the converter used Fairchild comparators and Texas Instruments circuits in the decoder. The logic level converter circuit uses a transistor and a zener diode to shift the output levels from the comparator to make it compatible with the integrated circuits of the decoding network.

Also the operational amplifier needed to subtract the analog signal representing the five most significant bits from the analog input is simply the one found in the output stage of the D/A converter.

The total conversion time of this particular design is quite small. Initially, the incoming analog signal is fed into the sample-and-hold circuit. The complete acquisition and setting time of this circuit, within 5mv of the signal, is less than 200 nanoseconds. The comparators, working simultaneously, take less than 40 nanoseconds and

the level shifters and 5-bit encoder together take 50 nanoseconds. Therefore, less than 300 nanoseconds after the initial sample pulse, the five most significant bits are determined. The D/A conversion and the subtraction of that result from the input signal is completed in 200 nanoseconds and the last four bits can be determined in 80 nanoseconds. The complete conversion time is, at a maximum, less than 580 nanoseconds. In applications where the analog signal is not changing continuously (i.e., it remains constant for at least the time it takes to perform the A/D conversion) and the sample-and-hold circuit is not needed, conversion rates of over 3 MHz can be achieved.

3. TECHNICAL DESIGN

3.1 Sample-and-Hold Circuit

The requirements for the sample-and-hold circuit are: 1) acquisition time less than 50 nanoseconds; 2) hold-time greater than 1 μsecond; 3) maximum change of stored or held voltage = 5mv; 4) analog voltage to be stored is sinusoidal and varies between 0 and +5.000 volts.

The sample-and-hold circuits investigated fall mainly into three categories, all of which have to do with storing voltage on a capacitor. The first as shown in Figure 10a is an exponential charge method. This method was the simplest to realize in terms of hardware. The switch used was a diamond gate (see D.C.S. report #188 for further details). The purpose of the resistor was to limit the current in the switch to a maximum of 10ma. The amplifier on the output is used merely as a buffer. Though this method worked, it lacked sufficient speed and accuracy. To meet the requirements stated previously, a small capacitor was needed, and that was the reason for many problems which arose.

The second method investigated is shown in Figure 10b. Here a controlled constant current source is switched on by a pulse and switched off when a comparator indicates the correct voltage is on the holding capacitor. Problems originated immediately in timing and turn-off transients.

In Figure 10c the third and final method is shown. This circuit consists of a holding capacitor, an amplifier, and a slightly modified "Vista Gate." The "Vista Gate" is a fast analog gate with current gain (for further details on the "Vista Gate" see D.C.S. Quarterly Report for

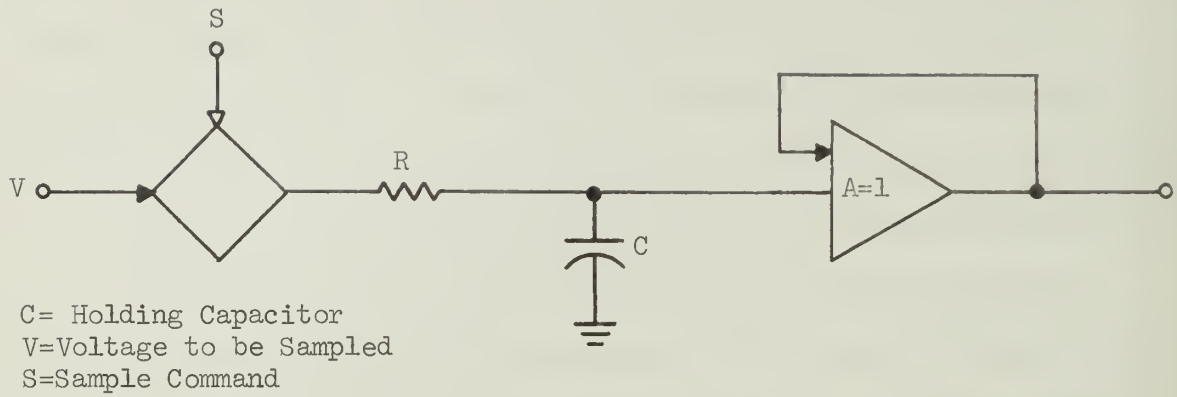


Figure 10a. Sample and Hold Circuit - Type I.

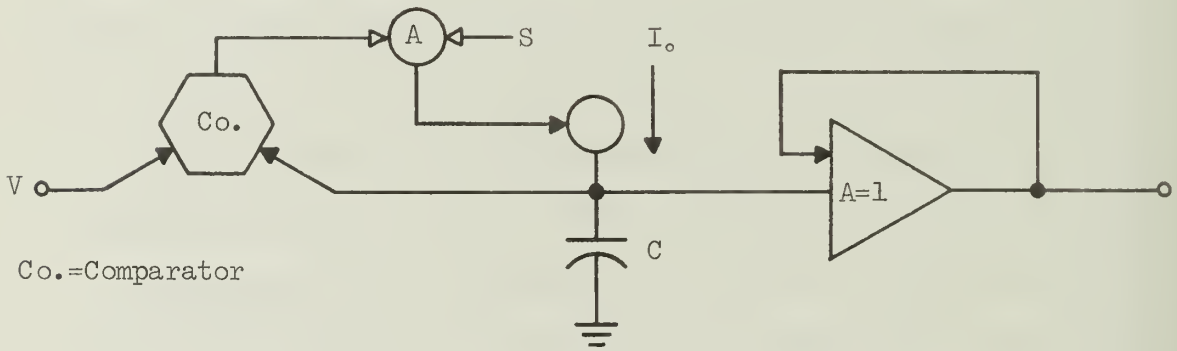


Figure 10b. Sample and Hold Circuit - Type II.

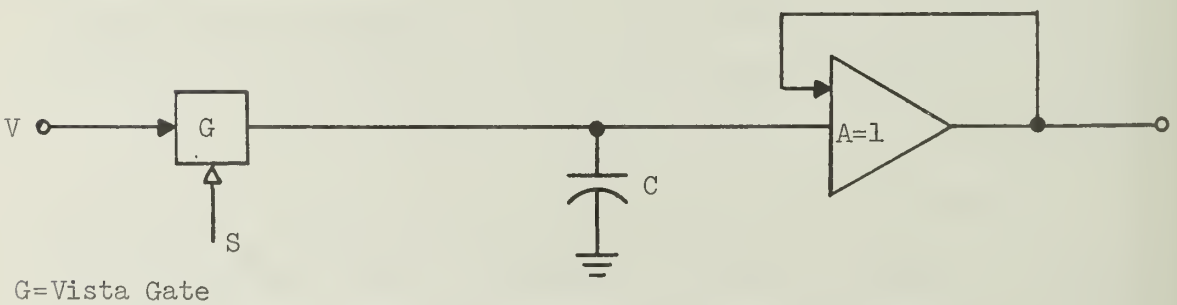


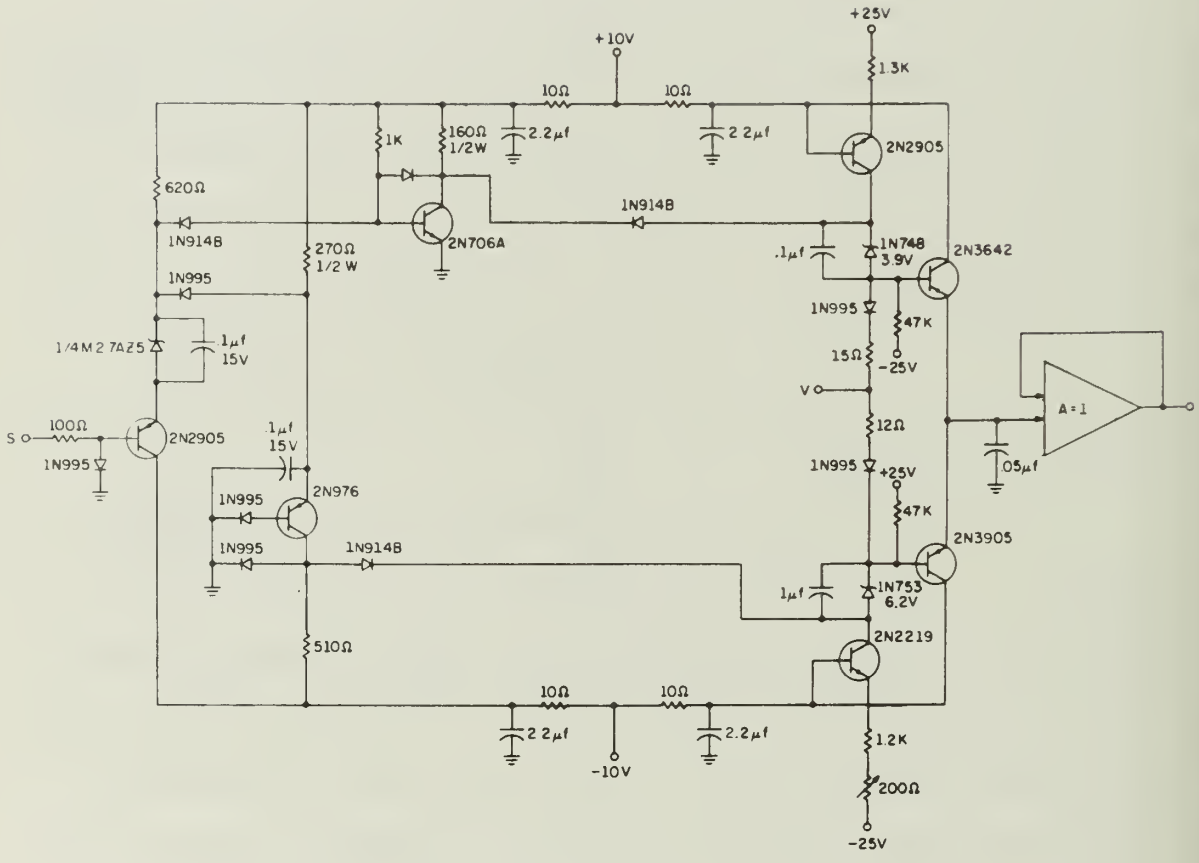
Figure 10c. Sample and Hold Circuit - Type III.

October, November, December, 1967). Basically, the operation of this circuit is simple. The voltage is continually fed onto the holding capacitor through the open "Vista Gate." When a sample pulse occurs, the gate is closed and the desired voltage is held on the capacitor. One immediate advantage to this method is that it is faster than the previous two because the voltage to be sampled is already on the capacitor when the sample pulse occurs. The speed with which the correct voltage is attained is important because it is necessary to wait until all transients have died down below 5mv before using the sampled voltage. A problem that arose was the phase delay of the analog signal through the gate and the speed at which the gate turned off. This was overcome by adjusting the time when the sample pulse closed the gate so that the output would be correct. The entire circuit is detailed in Figure 11.

3.2 Comparator Circuit

A comparator is similar to a differential-input operational amplifier. In fact, operational amplifiers are frequently used as comparators. However, in many applications, the comparator is expected to recover rapidly from saturation, which is its normal operating state. Additionally, the large output voltage swing desired for operational amplifiers is often a disadvantage when the comparator is used to drive low-level logic circuits. The comparator described is designed to overcome the limitations of operational amplifiers in this application. It features extremely fast recovery from saturation and an output which is compatible with practically all integrated logic forms.

The operation of the comparator can be explained using the simplified schematic in Figure 12. A differential input stage (Q_1 and Q_2)


+25V
+10V
1.3K
10Ω
10Ω
1K
160Ω 1/2W
2.2μf
2 2μf
2N2905
620Ω
1N914B
1N914B
2N706A
270Ω 1/2 W
.1μf
1N748 3.9V
2N3642
1N995
1N995
47K
1/4M2 7AZ5
1μf 15V
15Ω
-25V
V
A=1
S
100Ω
2N2905
1N995
.1μf 15V
12Ω
1N995
+25V
.05μf
2N976
1N995
47K
1N995
1N914B
2N3905
1μf
1N753 6.2V
510Ω
2N2219
10Ω
10Ω
2 2μf
2.2μf
1.2K
-10V
200Ω
-25V

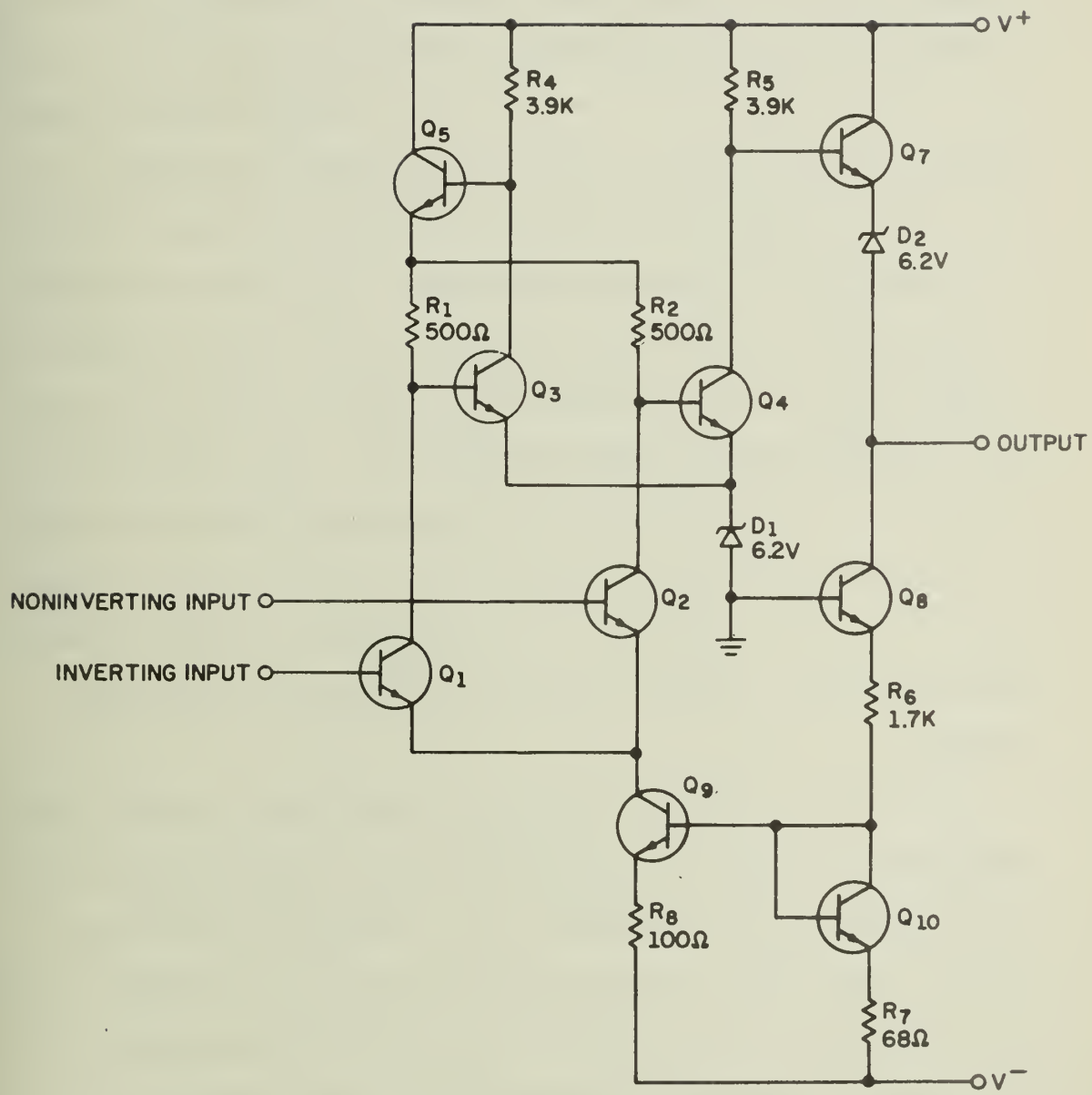


Figure 12. Simplified Schematic of Comparator.

is used for low offset. The emitters of the input stage are supplied from a current source (Q_9) to make their collector current insensitive to the common mode input voltage. A balanced second stage is also used: Q_4 is the actual second stage amplifier, while Q_3 provides balanced biasing for Q_4. The second stage can be understood by considering that Q_3 and Q_4 are identical transistors. Their bases are fed from a common voltage point, the emitter of Q_5, which keeps the input stage collector current out of R_4, through identical resistors (R_1 and R_2). When the input-stage collector currents are equal, the collector currents of Q_3 and Q_4 will be equal, so the second stage is balanced. Q_3 also functions as a unity-gain amplifier that inverts the output of Q_1 and combines it with the output of Q_2 at the base of Q_4. A single-ended output is obtained at the collector of Q_4. One feature of the second stage is that under balanced conditions, the single-ended output is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both Q_3 and Q_4 will increase such that the voltage on the collector of Q_4 remains constant.

An emitter follower is used at the output of Q_4 to give a high output-current capability. A zener diode (D_1) in the emitters of the second-stage transistors provides a large input-voltage range (the positive input-voltage limit is essentially equal to the voltage on the base of the second-stage transistors). An identical zener diode in the output emitter-follower (D_2) level shifts the output back to a level compatible with logic circuits. Q_8 isolates the output from the diode-compensated bias divider for the input-stage current source. Using the diode-connected transistor, Q_{10}, to compensate for the emitter-base

voltage of Q_9 permits the current source to operate with a small voltage drop across its emitter resistor, R_8. This gives an increased negative input-voltage limit.

The complete schematic of the comparator in Figure 13 shows the addition of Q_6 connected as a diode. This limits the positive output swing both to increase speed and to give compatibility with certain integrated logic families.

A mathematical analysis of the comparator operation shows that circuit performance is not affected by the loose component tolerances encountered with monolithic construction but depends on how well various parts match - something that is easily done in an integrated circuit. Since this matching can be maintained well over an extremely wide temperature range, the comparator is relatively insensitive to changes in operating temperature.

3.3 Bias Supplies for Comparator

The power supplies available for the Functional Encoding System are -25v, -10v, -5v, +10v, and +25v. The maximum ratings of the bias supplies for the comparator are -7v for the negative supply and +14v for the positive supply. While all the specifications on the comparator were given for bias supplies of -6v and +12v it was first thought that the -5v and +10v already available in the system could be used. However, it was determined that more accuracy could be obtained using the -6v and +12v supplies, so the power supplies shown in Figures 14 and 15 were designed.

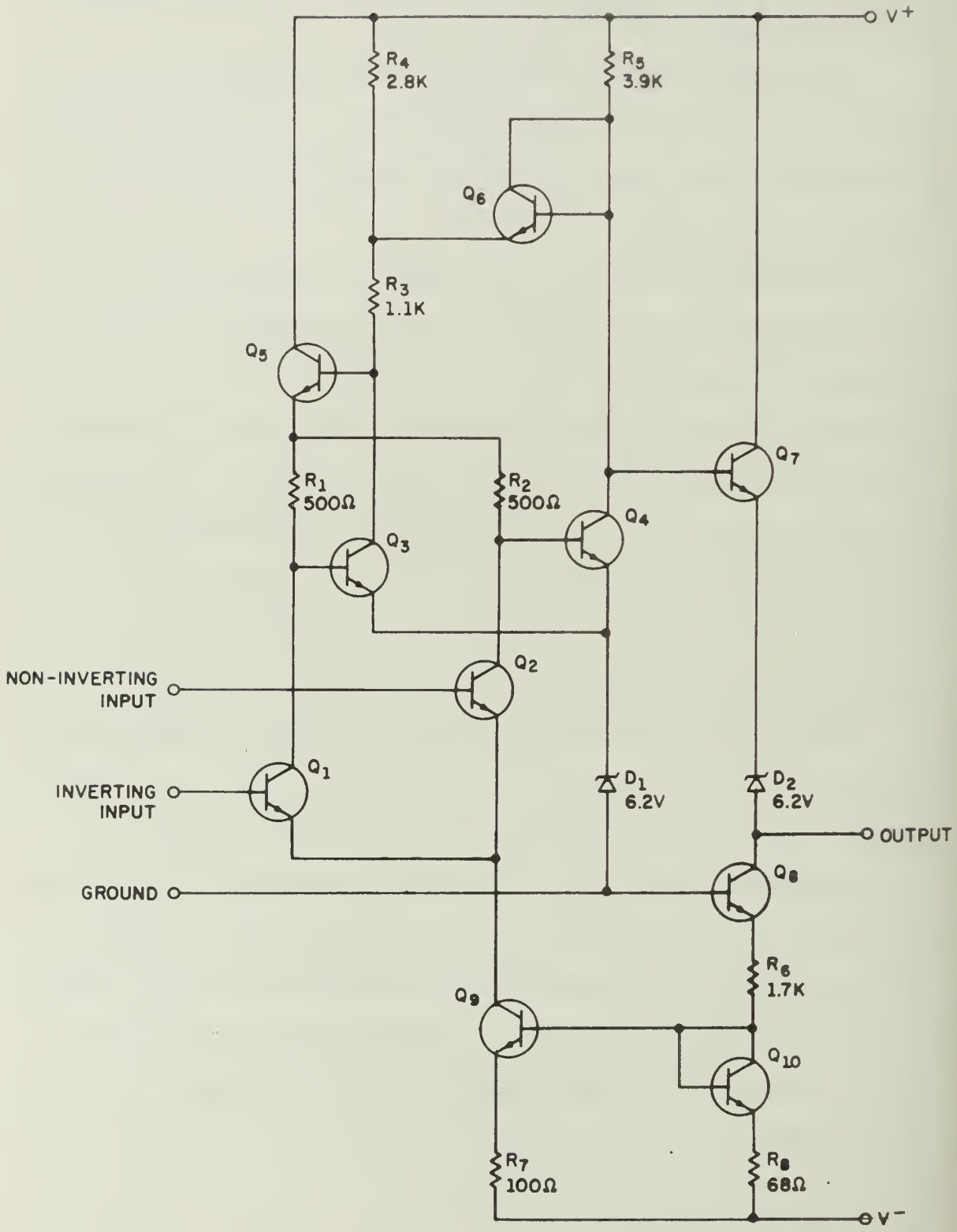


Figure 13. Schematic Diagram of Comparator.

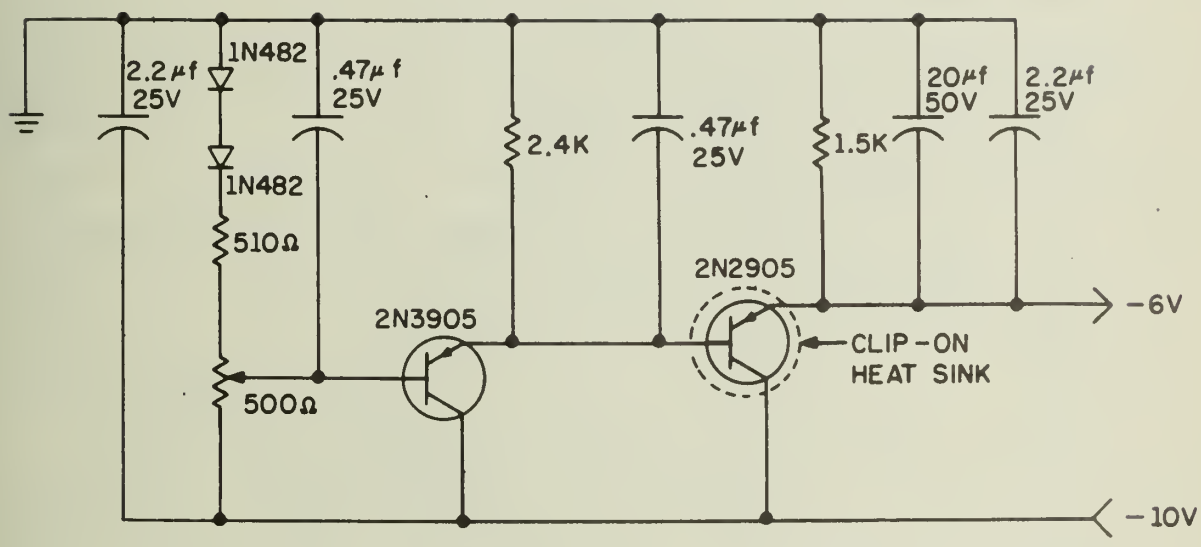


Figure 14. -6.0 Volt Power Supply.

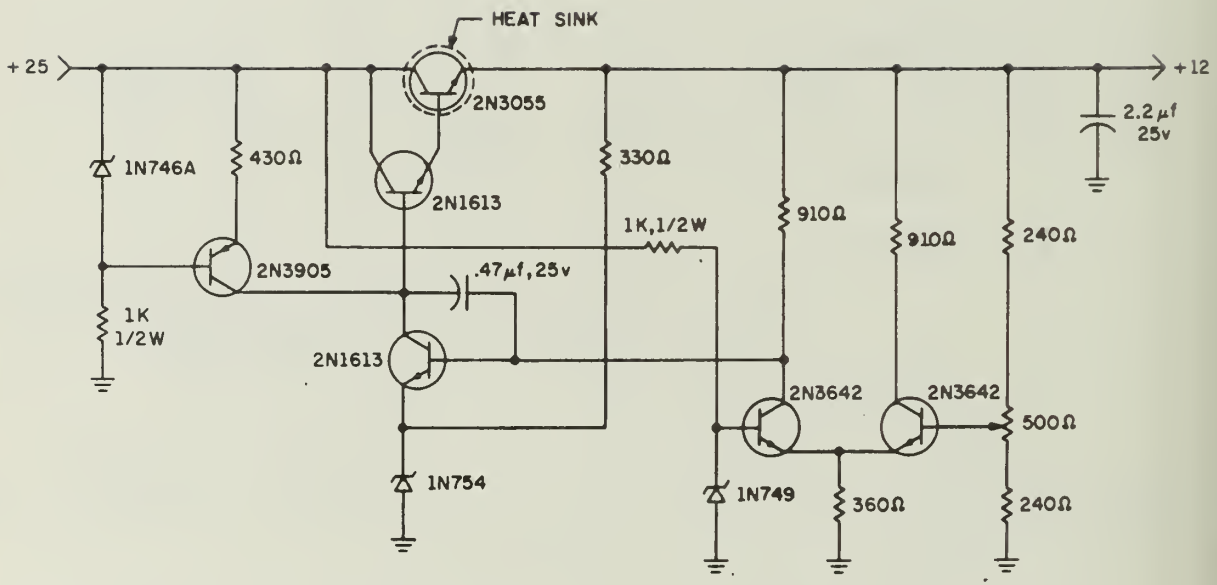


Figure 15. +12.0 Volt Regulator.

3.4 Resistor Chain

It has already been shown that after comparing an analog signal with 2^N-1 different, appropriate reference voltages and subsequently encoding the 2^N-1 digital outputs, an N bit binary representation of the analog signal could be accomplished. Therefore, to determine the five most significant bits 31 precision references are needed. Since the analog signal can be from 0v to 5.00v the references needed are (5.000v/32 = 156.25mv), (2 x 156.25mv = 312.50mv), ..., (31 x 156.25mv = 4.84375v). A resistor chain made up of 32 precision resistors was used for this purpose (see Figure 16). The total resistance of the chain was purposely chosen small enough to maintain a large standing current through the resistors. In this way, a change in the input currents to the comparators as the number of comparators that are on fluctuates, will not be large enough to cause a significant difference in any of the reference voltages. To further insure this fact the +5v supply was designed as a regulator with .5% regulation from no load to full load (see Figure 17).

Finally, after testing the circuit it was determined that the DC reference voltage tied to all 31 comparators became a source of unwanted oscillations. By connecting .47 μf capacitors between various points along the resistor chain and ground these oscillations were eliminated.

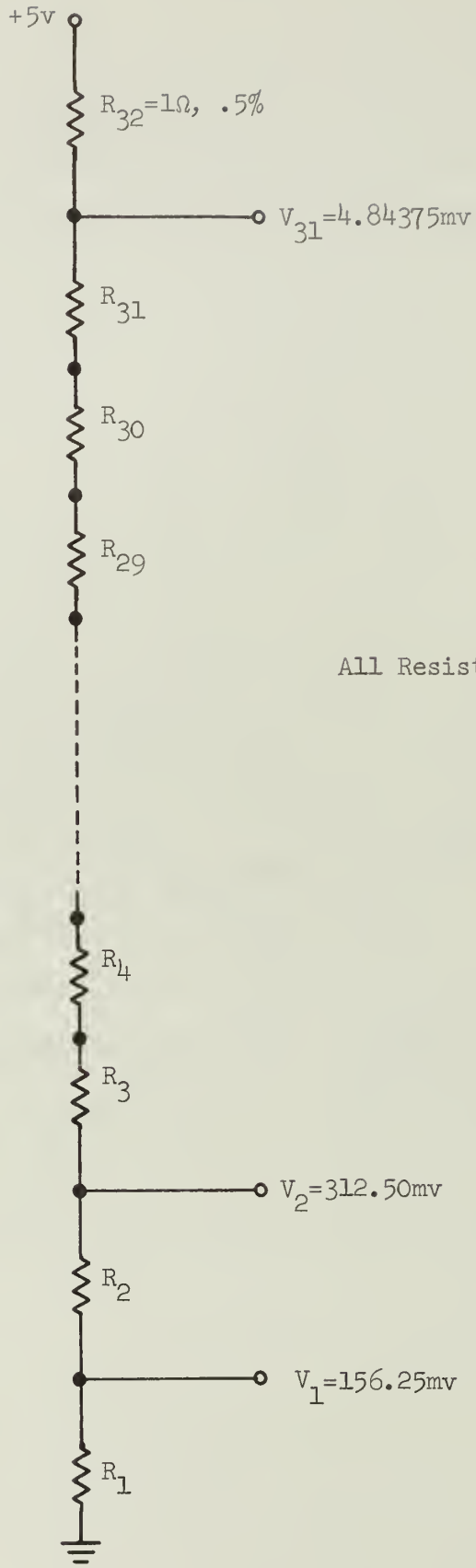


Figure 16. Resistor Chain.

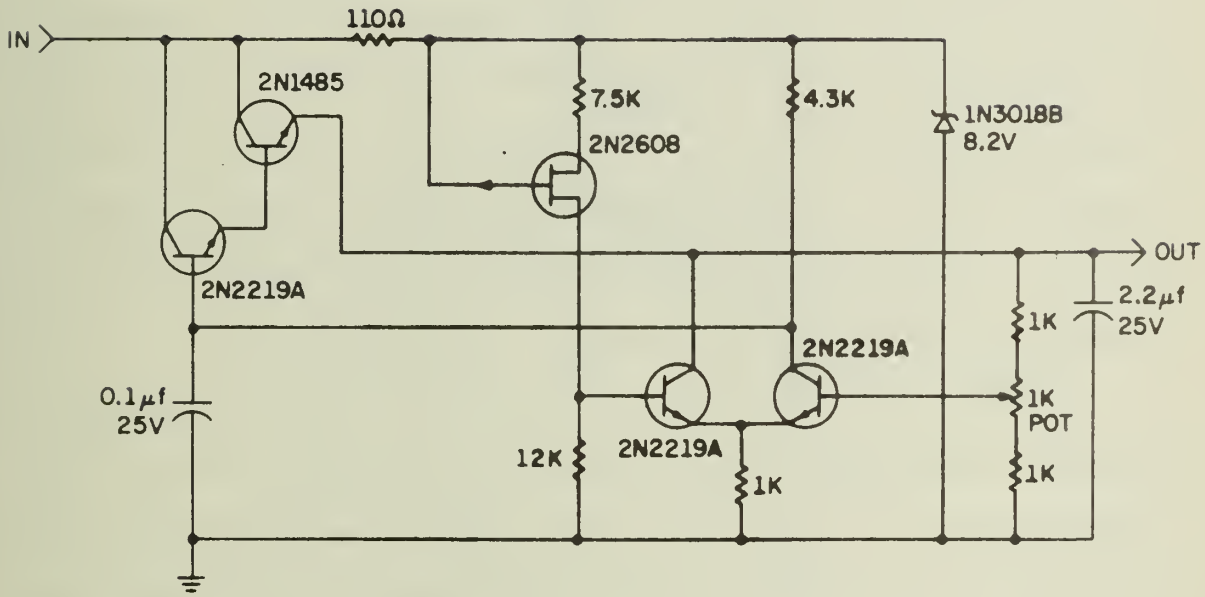


Figure 17. +5.0 Volt Regulator.

3.5 Level Shifting Circuit

When it was decided to use the comparators made by Fairchild Semiconductor Corporation it became necessary to build a circuit to make their outputs compatible with the Texas Instruments integrated circuitry. When the output of the comparator is a digital "1" it has a value of +3 volts. When it is a "0" it is -.5 volts. The digital "1" required by the Texas Instruments logic is from ground to -2.5 volts; the "0" is from -4.5 volts to -5.0 volts.

In order to keep the circuit as simple and as fast as possible only one transistor was used. This resulted in not only shifting the input but also inverting it so that a logical "1" becomes a logical "0" and vice-versa. To offset this change the precision reference and unknown analog signal inputs to the comparator are switched so that the comparator output is actually inverted. Therefore, after the second inversion of the 31 level shifting circuits the true output appears ready to be encoded into the five most significant bits.

Referring to Figure 18 it is seen that an input of +3 volts (a Fairchild logical "1") turns the transistor on, yanking the top of the zener diode down to just above +1 volt. Due to the biasing then, there is a 5.1 volt drop across the zener diode making the output just above -5.0 volts (a Texas Instruments logical "0"). An input of -.5 volts (a Fairchild logical "0") leaves the transistor off and therefore a standing current of about 12ma flows through the 510 ohm resistor. The top of the zener diode is at approximately +4.0 volts and the output is approximately -1.0 volts (a Texas Instruments logical "1").

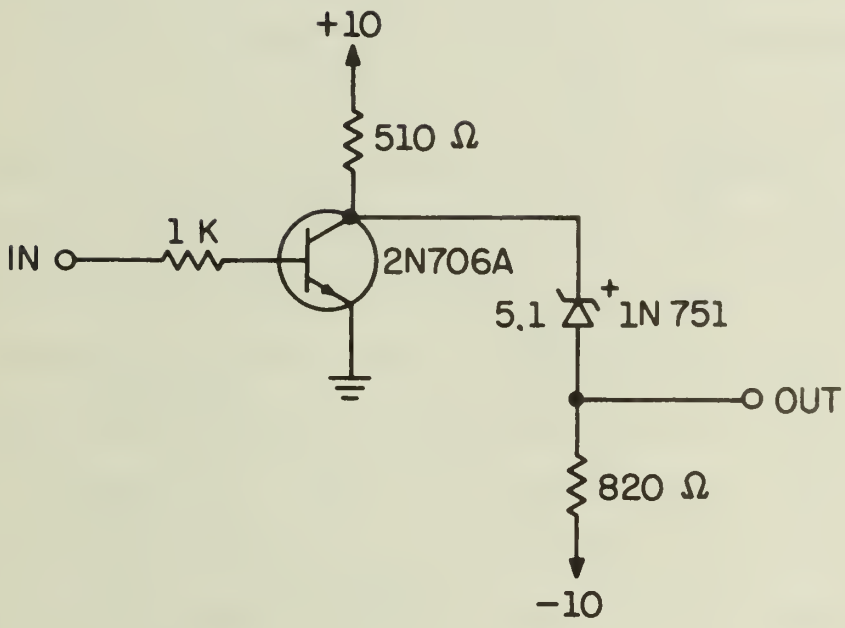


Figure 18. Logic Level Converter.

3.6 Decoding Network

The decoding network simply has to take the digital results of comparing an analog signal with 31 reference levels and code them into 5 bits of information. For example, the most significant bit determines whether the input is greater than or less than +2.5v so that to obtain the most significant bit one would just have to look at the output of the comparator with a reference voltage of +2.5v. For the second most significant bit the task is a little harder. That bit is a logical "1" if the input is between +1.25v and +2.5v or if the input is greater than +3.75v. Therefore, to determine the second most significant bit, a combination of three comparisons is needed - with reference voltages +1.25v, +2.5v, and +3.75v.

The entire decoding network for the five most significant bits is shown in Figure 19. The logical circuits used are two and four-input "nand" gates and four and eight-input "and-or-invert" gates. The "nand" gate "ands" all its inputs and then inverts the result (see Figure 20a). Therefore, to obtain a logical "0" all inputs to a "nand" gate must be logical "1's"; if any input to a "nand" gate is a logical "0", the output automatically is a logical "1". The "and-or-invert" gate pairs off, then "ands" the inputs (into two or four pairs depending upon which size gate is used), "ors" the pairs together, and finally inverts the result (see Figure 20b). To obtain a logical "0" then, both members of one of the pairs must be a logical "1"; if no pair has both inputs at a logical "1", the output automatically is a logical "1".

After all five bits are determined they are gated into five D-type, edge-triggered flip-flops which not only gives the information to the D/A converter, but serves as an output register as well (see Figure 20c).

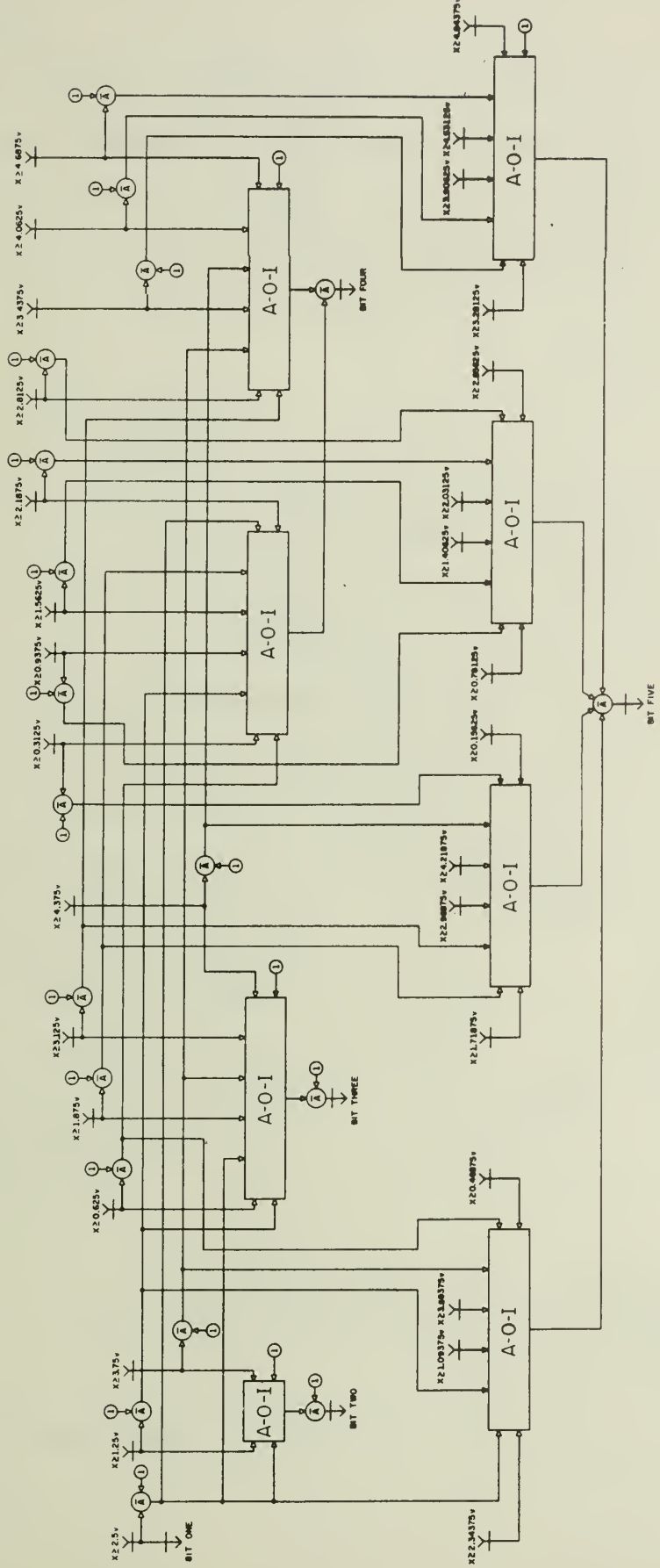


Figure 19. Decoding Network.

Figure 20a. Nand Gate.

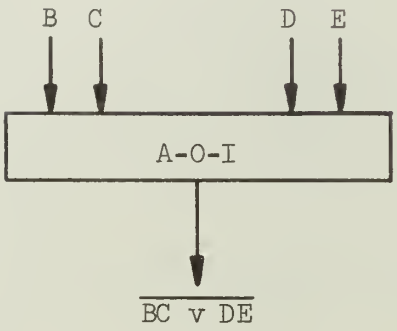
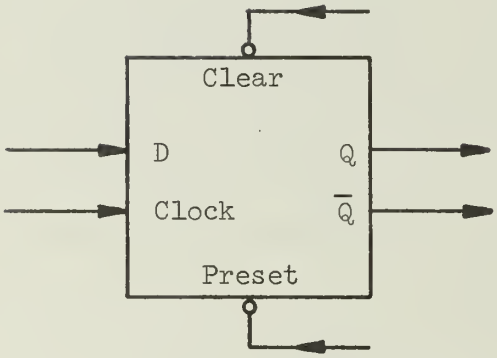


Figure 20b. And-Or-Invert Gate.



Truth Table

t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
0	0	1
1	1	0

a) t_n=bit time before clock pulse

b) t_{n+1}=bit time after clock pulse

1) Low input to clear sets Q to logical "0"
2) Low input to preset sets Q to logical "1"
3) Clear or preset inputs dominate regardless of clock and D inputs

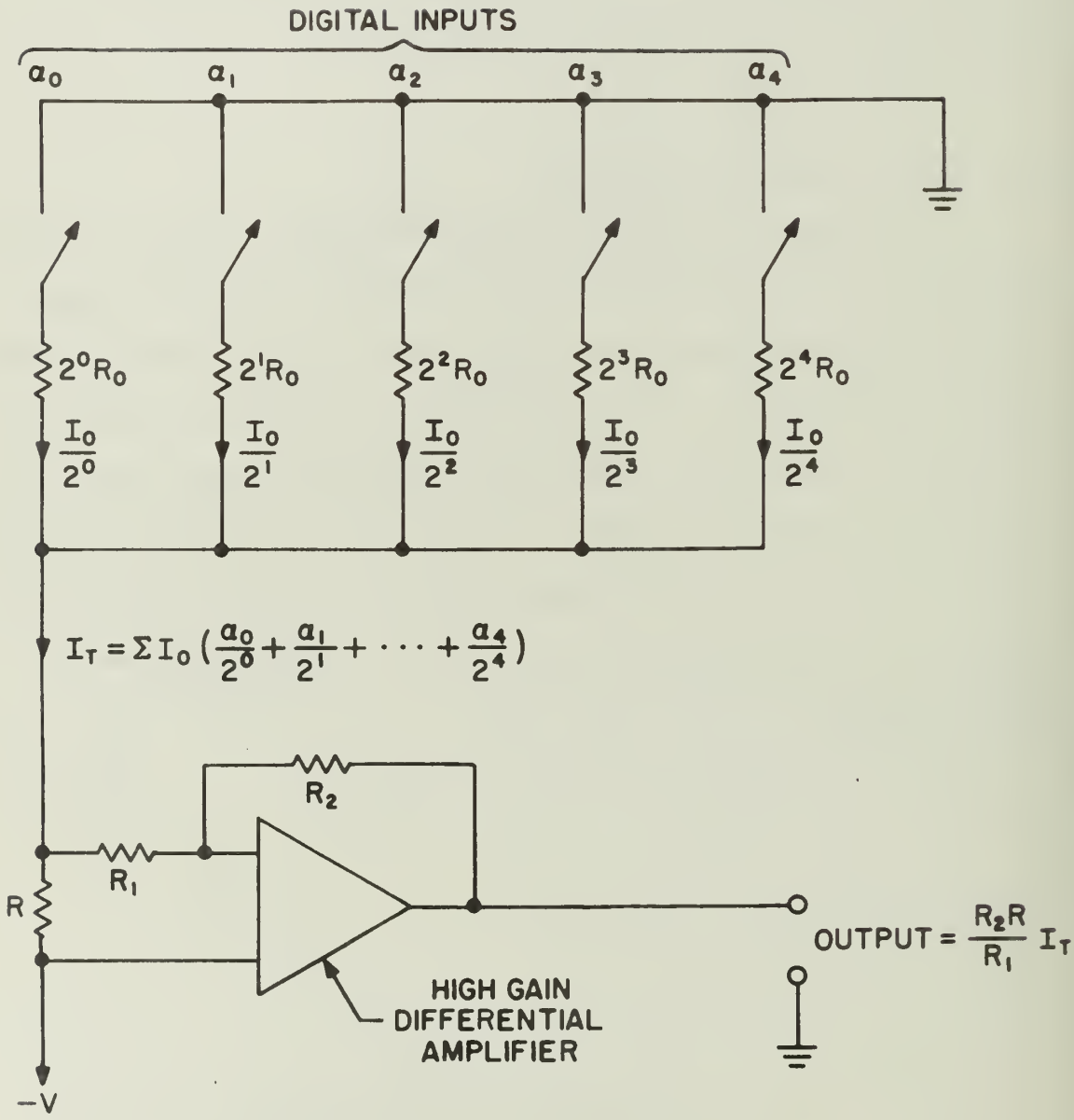
Figure 20c. D-Type Edge-Triggered Flip-Flop.

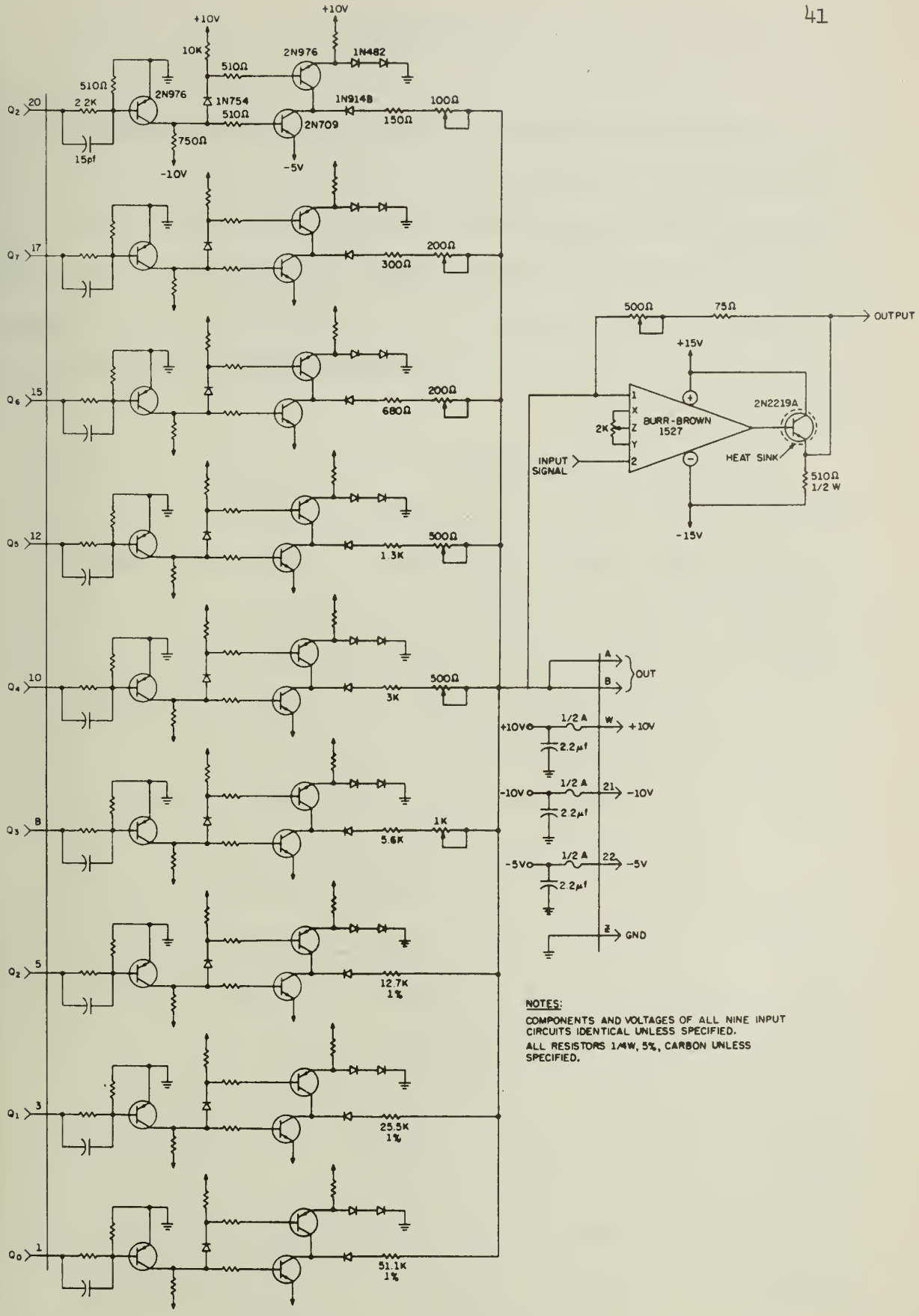
3.7 D/A Converter

After the five most significant bits are clocked into the register, the next step is to construct an analog signal corresponding to that binary number. For the basic scheme of the 5-bit D/A converter which does that, see Figure 21. Figure 22 shows the actual circuit configuration.

3.8 The Four Least Significant Bits

To determine the four least significant bits, a process identical to finding the five most significant bits is used. The analog signal remaining after the subtraction in the output stage of the D/A converter, appropriately amplified, is the input to this section of the converter. The signal is amplified so that the same reference voltages used in the first section could be used again. Though only 15 comparators are needed in this process, the level shifters, comparators, decoding network, and register are the same circuits which have been described previously in this chapter.


DIGITAL INPUTS
a_0
a_1
a_2
a_3
a_4
2^0R_0
2^1R_0
2^2R_0
2^3R_0
2^4R_0
$\frac{I_0}{2^0}$
$\frac{I_0}{2^1}$
$\frac{I_0}{2^2}$
$\frac{I_0}{2^3}$
$\frac{I_0}{2^4}$
$I_T = \Sigma I_0 \left(\frac{a_0}{2^0} + \frac{a_1}{2^1} + \cdots + \frac{a_4}{2^4}\right)$
R_2
R_1
R
HIGH GAIN
DIFFERENTIAL
AMPLIFIER
$-V$
OUTPUT = $\frac{R_2R}{R_1} I_T$



NOTES:

COMPONENTS AND VOLTAGES OF ALL NINE INPUT CIRCUITS IDENTICAL UNLESS SPECIFIED.

ALL RESISTORS 1/4W, 5%, CARBON UNLESS SPECIFIED.

Figure 22. D/A Converter.

4. CONCLUSION

Integrated circuits already have a strong position in A/D technology but chiefly in programming or logic (for example, the Decoding network). As recently as late 1967, however, integrated circuits have not been extensively used in the analog area. The use of the integrated circuit comparator in the A/D converter design detailed heretofore shows that the 100 KHz converters generally used now can be improved significantly.

Though it is not necessary for use in the Functional Encoding System, the A/D converter design outlined in this paper could function as fast as 3 MHz. There is logic available now which has propagation delay times one-half as large as those in the logic of the A/D converter. Furthermore, a large part of the conversion time is made up of the time it takes for the sample-and-hold circuit to settle down. Problems encountered in the area of matching impedances while operating at high speeds ("microwave plumbing"), ground loops, and ground noise can be solved by using the techniques of time-domain reflectometry. This would result in much less of a problem from transients throughout the circuit due to very fast turn-off times. It is not impractical to expect that the settling time of the sample-and-hold circuit could be reduced from 200 nanoseconds to 100 nanoseconds. Finally, there is the time for the D/A conversion. In this case the fastest of the available operational amplifiers is used to assure as much accuracy as possible. However, in the event that some accuracy may be sacrificed for speed, lower gain-higher speed integrated circuit operational amplifiers may be employed with a subsequent reduction in the D/A conversion time.

There is no denying that this design technique has inherent problems. Great care has to be taken when employing the comparators in large numbers under such conditions, and at such speeds. For example, it is suggested that the output of each comparator be as far away from the inputs as practicality permits. It has been demonstrated, however, that the use of the high-speed integrated circuit comparator makes practical some of the very fastest A/D conversion techniques, which, until now, have just been theory.

LIST OF REFERENCES

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. October-December, 1966.

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. January-March, 1967.

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. April-June, 1967.

"Quarterly Technical Progress Report", (Hardware Systems Research), Department of Computer Science, University of Illinois, Urbana, Illinois. July-September, 1967.

The Digital Logic Handbook, Digital Equipment Corporation, 1966.

Notes on A/D Conversion Techniques, Susskind, Alfred K., The M.I.T. Press, 1957.

"Special Report on A/D Converters", by George Flynn, Electronic Products, 1967.

"The Operation and Use of a Fast Integrated Circuit Comparator", by R. J. Widlar, Fairchild Semiconductor, Inc., 1967.